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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/939,752	08/28/2001	Masaki Komaki	024016-00014	3840

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[REDACTED] EXAMINER

NGUYEN, JOSEPH H

[REDACTED] ART UNIT [REDACTED] PAPER NUMBER

2815

DATE MAILED: 05/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/939,752	KOMAKI, MASAKI	
	Examiner	Art Unit	
	Joseph Nguyen	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 25 March 2003.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-22 is/are pending in the application.

4a) Of the above claim(s) 12-18 is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-11 and 19-22 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 28 August 2001 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) <input type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

Claim Objections

Claims 1 and 8 are objected to because of the following informalities: --form—in line 5 of claim 1 and in line 5 of claim 8 should be –formed--. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless —

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 21 is rejected under 35 U.S.C. 102(b) as being anticipated by Fudanuki et al

Regarding claim 21, Fudanuki et al discloses on figure 10B a semiconductor integrated circuit comprising a first hierarchy where a plurality of fundamental cells and a plurality of connector terminals 610 wherein metal wirings 516 other than power supply wirings are formed; and a second hierarchy provided above the first hierarchy wherein fixed power supplies Vss are formed; wherein the plurality of fundamental cells and the fixed power supplies are connected via the plurality of connector terminals.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-11, 19- 20, 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over figures 13 of acknowledged prior art (APA) in view of Fudanuki et al.

Regarding claim 1, (APA) discloses a fundamental cell used as a basic unit in the layout of a semiconductor integrated circuit device and being in a stage after metal wiring is formed comprising connector terminals 101 to be connected to upper wiring layers M2. (APA) does not disclose no fixed wiring for commonly wiring between fundamental cells in a hierarchy where fundamental cells being formed. However, Fudanuki et al discloses on figure 10A no fixed wiring for commonly wiring between fundamental cells in a hierarchy where fundamental cells being formed. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify (APA) by having no fixed wiring for commonly wiring between fundamental cells in a hierarchy where fundamental cells being formed for the purpose of improving the density integration of the semiconductor device as taught by Fudanuki et al (col. 12, lines 30-40).

Regarding claims 2-7, (APA) and Fudanuki et al together disclose the structure set forth in claims 2-7.

Regarding claim 8, (APA) discloses substantially all the structure set forth in the claimed invention except no fixed wiring for commonly wiring between fundamental cells in a hierarchy where fundamental cells being formed. However, Fudanuki et al discloses on figure 10A no fixed wiring for commonly wiring between fundamental cells in a hierarchy where fundamental cells being formed. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify (APA) by having no fixed wiring for commonly wiring between fundamental cells in a hierarchy where fundamental cells being formed for the purpose of improving the density integration of the semiconductor device as taught by Fudanuki et al (col. 12, lines 30-40).

Regarding claim 22, (APA) discloses substantially all the structure set forth in the claimed invention except no fixed wiring for commonly wiring between fundamental cells in a plane where fundamental cells being formed. However, Fudanuki et al discloses on figure 10A no fixed wiring for commonly wiring between fundamental cells in a hierarchy where fundamental cells being formed. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify (APA) by having no fixed wiring for commonly wiring between fundamental cells in a plane where fundamental cells being formed for the purpose of improving the density integration of the semiconductor device as taught by Fudanuki et al (col. 12, lines 30-40).

Regarding claims 9-11, 19 and 20, (APA) and Fudanuki et al together disclose the structure set forth in claims 9-11, 19 and 20.

Response to Arguments

Applicant's arguments filed on 3/25/2003 have been fully considered but they are not persuasive.

With respect to claims 1 and 8, applicant argues that Fudanuki does not disclose no fixed wiring for commonly wiring between fundamental cells in a hierarchy where fundamental cells are formed. However, Fudanuki clearly teaches, "the gate array basic cells GC are arranged in the empty spaces 33 on the arrangement pattern of the standard cells SC's. Such advantage can be accomplished that integration density can be improved by spreading the channelless standard cells all over the surface and wiring design can be made easy because no fixed wiring area remains" (col. 12, lines 27-40). It is clear that Fudanuki discloses no fixed wiring in a hierarchy where fundamental cells are formed. Also, there is no disclosure of so-called fixed wirings anywhere in Fudanuki thereto. As such, with a strong motivation provided by Fudanuki, the combination of figure 13 of (APA) and Fundanuki would clearly disclose all the structures set forth in now amended claims 1 and 8.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Nguyen whose telephone number is (703) 308-1269. The examiner can normally be reached on Monday-Friday, 7:30 am- 4:30 pm

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 308-7382 for regular communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JN
May 19, 2003



EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800